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for

POWER LINE ARRANGEMENT FOR ELECTROLUMINESCENCE DISPLAY DEVICES

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POWER LINE ARRANGEMENT FOR ELECTROLUMINESCENCE DISPLAY DEVICES

BACKGROUND

[0001] The present disclosure relates generally to electroluminescence (EL) display devices, and more particularly to the design of the voltage power lines used for the display elements of the electro-optical display devices and the like.

[0002] Typical electroluminescence (EL) display devices comprise of a plurality of light emitting diode (LED) elements (pixels) which are connected and arranged in a matrix, row-column array construction. Using organic light emitting diode (OLED) pixels as an example, each pixel is equipped with a switching and a driving circuit, usually comprised of capacitors and thin film transistors (TFTs) connected to scan, data and voltage power lines. The combination of these circuits and lines serve to provide display information and emission for each OLED pixel. Image display information is sent to the matrix of OLED pixels via routings of the scan and data lines that are connected to drive each OLED pixel-circuit set. Power lines provide the positive (Vdd) and negative (Vss) voltages required to power the emission of the driven EL diodes. Specifically, the Vdd power supply is connected to the driving anodes of the OLED elements and the Vss power supply is connected to the elements' cathodes.

[0003] The three line types, scan, data and power, are comprised of conducting metal alloys. Conducting metal alloys featuring low resistivity material property are used as the lines to help maintain low operating resistance minimizing the voltage

drop effects due to the material properties of the lines. Resistance may be defined by the following resistance equation for a solid rod or line material, $\mathbf{R = \rho * L / A}$. The equation utilizes the resistivity constant ρ for the given material, **L** the length of the rod or line material, and **A** the cross-sectional area of the rod or line material. The relationship of resistance to voltage is described by Ohm's Law, $\mathbf{V = R * I}$, where the voltage (**V**) drop across a given material for a passing current (**I**) is dependant upon the electrical resistance (**R**) of the conducting material. The construction of the display device's matrix array unfortunately results with metal line routings of different lengths and cross-sectional areas to each OLED pixel-circuit set from the originating scan, data, and or power sources. The varying routing lengths of the metal lines effectively impose varying in-line resistance values onto the various OLED pixel-circuit sets. As result, the delivered voltage level to the OLED pixels and their associated circuits may not be the same for all OLED pixel locations of the EL display device's matrix array.

[0004] Figs. 1a and 1b are top views of two typical OLED display devices illustrating the distribution and routings of the Vdd and Vss power supply lines throughout the OLED display device. These OLED display devices are of the bottom-emitting type, where the OLED emit in the direction originating from the EL material layer, through the OLED display elements' Vdd anode material and the device substrate.

[0005] Fig. 1a shows the OLED display device 100 comprising of a device substrate 102 and an active OLED pixel display area 104. The two major power bus lines for supplying power to the OLED EL elements are shown as the Vdd bus line 106 and the Vss bus line 108, located adjacent to the active OLED pixel area 104. As viewed by Figs. 1a and 1b, the Vss bus line 108 connections to the EL display

elements of the active OLED pixel area 104 are accomplished with line routings (not shown) from the Vss bus line 108, underneath the active OLED pixel display area 104, to the OLED EL display elements. Connections from the Vdd bus line 106 to the OLED display elements of the active OLED pixel display area 104 are routed through the smaller Vdd lines 110 of Figs. 1a and 1b. Note that the routing across the active OLED pixel area 104 for Fig. 1a is in a row alignment/arrangement, while the Vdd lines 110 of Fig. 1B is shown in a column alignment/arrangement. Each Vdd line 110 layout provides a path from their main Vdd bus line 106 to the individual OLED pixel display elements of the active OLED pixel area 104. It is also noted that the lengths of the Vdd and Vss power supply lines to each EL element location within the active OLED pixel area 104 are not equal. In other words, the total metal volume used for delivering power to each EL element location through the various metal buses and lines are not equal. This inequality of conductance paths leads to varying resistances applied to the power line routings such that varying voltages are delivered to the individual EL display elements. Further, due to the voltage drop along the line, the pixels of the display device at the far end of the supply lines 110 away from the power supply bus line 106 suffers from a relatively lower power supply level, thereby degrading the display quality.

[0006] Fig. 2 illustrates a basic cross-sectional view of an OLED device 200 within the active OLED pixel area. The device substrate 202 is shown at the bottom, with the OLED anode 204 located on the device substrate. The OLED emissive EL element 206 is shown attached to the anode 204. The cathode 208 is also attached to the OLED emissive EL element 206 on the side opposite than that of the attached anode 204. It is noted that there are other dielectric material layers and structures that may be present and located between adjacent anode 204 and cathode 208, and between certain areas of the OLED EL emissive element 206 and the adjacent metal

layers, for the purpose of insulating the conducting lines and certain circuit component features from each other. These dielectric layers and structures are not shown on the Figs 1a, 1b and 2, to help simplify and emphasize the inventions disclosed.

[0007] Referring back to Figs. 1a and 1b, the metal power supply bus lines, Vss lines 108 and Vdd lines 106 and 110 feature routing layouts that are two-dimensional, with no like lines in any vertically overlapping or multi-layered arrangement. The cross-sectional view of Fig. 2 also shows the non-overlapping arrangement. The cathode 208 is shown to have at least one vertical step, from one height to another within it's routing, but it is noted that the routing with the vertical step does not feature any overlap or multi-layering arrangement of the metal line.

[0008] Advanced EL display devices feature high performance image display qualities taking into consideration of factors such as brightness, contrast, resolution, colors, flicker, distortion and linearity. In addition, advanced EL display devices may feature high operational refresh speeds, as well as low overall power consumption. Varying and unbalanced levels of voltage between the OLED pixel locations of such advanced EL display devices may counteract and cause undesired effects upon the image display qualities, as well as to the operational speeds and power consumption. While efforts have been made to utilize metal lines featuring low resistivity material, more focus is needed upon the other contributing factors (e.g., length **L** and cross-sectional area **A**) to lower the resistance (**R**) of the metal lines.

[0009] What is desirable is an improved method for the design and routing of power supply lines that features lower resistance throughout the different routings and lengths to the individual OLED pixel emission locations since lower resistance

metal lines would provide lower magnitudes of voltage drops to the OLED pixel emission elements.

SUMMARY

[0010] In view of the foregoing, this disclosure provides an improved method for delivering power to display devices for avoiding degraded display quality due to the voltage drop across the power supply lines.

[0011] In one example, a light emission display device with improved power supply line arrangement and method for forming the same is disclosed. The device has a cathode layer, an insulating layer covering at least one portion of the cathode layer, and a power supply plane formed on the insulating layer overlapping the covered portion of the cathode layer to form a predetermined area under which a display area is located, wherein the power supply plane provides even distribution of power to the active display area.

[0012] The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIGs. 1a and 1b illustrate top views of two typical OLED display devices illustrating the distribution and routings of the Vdd and Vss supply lines within the OLED display device.

[0014] FIG. 2 illustrates a basic cross-sectional view of the OLED display pixel area.

[0015] FIG. 3 illustrates a cross-sectional view of the OLED Vdd line and the Vss line routings within the active OLED pixel areas of an OLED display device in accordance with one example of the present disclosure.

[0016] FIGs. 4a and 4b illustrate top views of several material layers of a display device in accordance with two examples of the present disclosure.

[0017] FIGs. 5a and 5b are top views of two OLED display devices illustrating two examples of the distribution and routings of the Vdd and Vss supply lines in accordance with the present disclosure.

DESCRIPTION

[0018] The present disclosure describes an improved method for arranging power supply lines in order to reduce the voltage drop across the power supply lines used within EL display devices. The disclosed method features an improved metal line routing layout to provide power nearer and closer to the EL display emissive elements such that the voltage drops experienced by the display elements are lowered and minimized. The utilization of a power supply plane to improve the delivery of power requires no or minimal change to the effective width and pitch of the device circuit lines, thus requiring no or little change to the two-dimensional, x-y layout of the associated circuits as well as to the overall size of the of EL display devices.

[0019] Fig. 3 illustrates a cross-sectional view of the OLED Vdd line and the Vss line routings within the active OLED pixel areas of an OLED display device with the

power lines arranged in a layout in accordance with the present disclosure. The OLED display pixel shown by Fig. 3 is of the bottom-emitting type, as the OLED emission occurs in the direction originating from the EL material layer, through the OLED display element's Vdd anode material and the device substrate. The device substrate 302 is shown with an OLED anode 304 located on the device substrate. The EL element 306 is shown located attached to the anode 304. A cathode material 308 is connected to negative power supply or Vss through interconnections 309. The anode 304 in Fig. 3 may also be referred to the Vdd power line for this display pixel.

[0020] The disclosed method provides an additional dielectric layer 310 located on top of the cathode 308. This dielectric layer 310 serves to insulate the cathode 308 from another layer of Vdd power supply material or power supply plane 312, located on top of the dielectric layer. This layer of power supply plane 312 is electrically and physically connected to the anode 304 by power supply lines (or sometimes interconnections) 314 in a location near and adjacent to the OLED pixel's emissive EL element 306. In stead of relying on long metal power supply lines alone, the Vdd power supply plane 312 provides metal volume for conducting power voltage to the active OLED pixel areas, thus lowering the resistance and voltage drop experienced at each emissive EL element 306. The Vdd power supply plane 312 may be comprised of the same or similar metal alloy as that of the anode 304. In this example, the negative power supply or Vss line 309 and the positive power supply or Vdd line 304 are located in locations close to the EL element 306, but on two sides of it.

[0021] It is also noted that there may be other elements of display device such as other materials for insulating one conducting line from another. These elements are not shown here in order to simplify and emphasize the locations of the multi-

layered power supply arrangement, dielectric layer 310, and the via interconnection 314, with respect to the device substrate 302 and to the EL element 306.

[0022] Fig. 4a illustrates a top view of some material layers of the display device 400 in accordance with an example of the present disclosure. For illustration purposes, only the Vss power supply plane or cathode layer 402, the insulating dielectric layer 404 and the Vdd power supply plane 406 are shown, and other layers are ignored. The cathode layer 402 is formed first by using a predetermined mask in a photolithography process to define the boundaries thereof. Next, the insulating dielectric layer 404 is formed over the cathode layer 402, and then, the Vdd power supply plane 406 is provided over the insulating dielectric layer 404. Via interconnections 408 are shown to be constructed to connect the Vdd power supply plane with the anode of each pixel or power supply lines beneath. The cathode layer 402 can make connections to the Vss power bus line through interconnections 410.

[0023] Fig. 4b illustrates a top view of some material layers of the display device 400 in accordance with another example of the present disclosure. Similar to Fig. 4a, for illustration purposes, only the cathode layer 402, the insulating dielectric layer 404 and the Vdd power supply plane 406 are shown, and other layers are ignored. In this example, the three different layers of materials are formed with similar sizes. As such, a single photomask can be used for defining the boundaries of these layers in photolithography processes. For example, the cathode layer 402 is formed first by using a predetermined mask to define the boundaries thereof. Next, the insulating dielectric layer 404 is formed over the cathode layer 402 by shifting the same photomask toward left for a predetermined distance, and then, the Vdd power supply plane 406 is provided over the dielectric layer 404 with the photomask shifting toward left for another predetermined distance. These distances are

determined based on the overlapping area in the middle that is needed for the EL element and/or spaces available for constructing via interconnections. As shown, interconnections 408 can be constructed to connect the Vdd power supply plane with the power supply lines underneath. The cathode layer 402 can make connections to the Vss power bus line of the active OLED device through interconnections 410.

[0024] Referring now to Figs. 5a and 5b, there are top views of two OLED display devices illustrating two examples of the distribution and routings of the Vdd and supply lines in accordance with the present disclosure. The OLED display device 500 is shown comprising of a device substrate 502 and an active OLED pixel display area 504. A Vdd power bus line 506 supplies power to the OLED device is also shown. The Vss power bus line is intentionally not shown in this illustration as the arrangement for these two power supply lines can be the similar. The Vdd power bus line 506 is connected to the Vdd power supply plane 508, which forms various connections 510 to Vdd power lines 512 that supply the EL display elements with voltage. Since the Vdd power supply plane is a relative large area that covers at least a great portion of the display area, the connections 510 can be made on opposite sides of the display area so that there will be no uneven voltage distribution from one side to the other.

[0025] Fig. 5b illustrate another example of the present disclosure. The OLED display device 520 is shown comprising of a device substrate 522 and an active OLED pixel display area 524. A power bus line for supplying power to the OLED EL elements are shown as the bus line 526. The bus line 526 is connected to the power supply plane 528, which forms various interconnections 530 to power lines 532 that supply the EL display elements with voltage. Since the power supply plane

is large enough to cover at least a major portion of the display area, the interconnections 530 can be made on adjacent sides of the display area to form a power supply line mesh so that uneven voltage distribution will be avoided or reduced. It is further noticed that the power supply plane 528 does not have to be in any particular shape as long as it covers the area in which the interconnections are made. Although not shown, it is understood that there are other via interconnections for electrically and physically connecting the power supply lines 532 to each active EL pixel location.

[0026] The present disclosure provides an improved method for the reduction of the voltage drop effects experienced by the metal lines used within EL display devices. The disclosed method utilizing one or more power supply plane for delivering the power voltage to the EL display elements such that the voltage drops experienced by the display elements are lowered and minimized.

[0027] The disclosed power supply line arrangement and structures may be applicable for use upon the various metal line levels of the EL display device, including the scan, data, power and any other metal lines as well as for EL display elements of varying styles, including bottom-emitting and top emitting types.

[0028] The disclosed power supply line arrangement requires no or minimum change to the practical width and pitches of the set metal lines, thus adding no significant requirement for change to the two-dimensional, x-y layout of the associated circuits, as well as to the overall sizing of the EL display devices. The arrangements of the present disclosure may also be implemented into future as well as older display device technologies, not limited to organic and EL display devices. The benefits provide will allow for display devices of higher reliability, longer operational life and of better performance quality. Such improvements will translate

into significant cost improvements for a given production facility to maintain highly competitive cost and output advantages over other manufacturers of similar product devices.

[0029] The above disclosure provides many different embodiments or examples for implementing different features of the disclosure. Specific examples of components and processes are described to help clarify the disclosure. These are, of course, merely examples and are not intended to limit the disclosure from that described in the claims.

[0030] Although the invention is illustrated and described herein as embodied in a design and method for , it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the disclosure, as set forth in the following claims.